VERIFICATION OF TRANSLATION

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Title of the Invention: SOLID-STATE IMAGING APPARATUS AND METHOD FOR PRODUCING THE SAME

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At Osaka, Japan

Dated this 22/ 2/ 2005 (Day/Month/Year)

Signature of translator:

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JAPAN PATENT OFFICE

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[List of File Documents]

[Name of Document]	Patent Specification	1
[Name of Document]	Drawing	1
[Name of Document]	Abstract	1

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[Proof] Required

[Document Name] SPECIFICATION

[Title of the Invention] SOLID-STATE IMAGING APPARATUS

[Claims]

[Claim 1] A solid-state imaging apparatus, comprising:

a plurality of photosensitive cells disposed in a matrix in a photosensitive region on a semiconductor substrate; and

driving means provided for driving the plurality of photosensitive cells,

wherein each of the photosensitive cells includes:

a photodiode formed to be exposed on a surface of the semiconductor substrate, for accumulating signal charge obtained by subjecting incident light to photoelectric exchange;

a transfer transistor formed on the semiconductor substrate, for transferring the signal charge accumulated in the photodiode;

a floating diffusion layer formed on the semiconductor substrate, for temporarily accumulating the signal charge transferred by the transfer transistor; and

an amplifier transistor formed on the semiconductor substrate, for amplifying the signal charge temporarily accumulated in the floating diffusion layer,

characterized in that a source/drain diffusion layer provided in the amplifier transistor is covered with a salicide layer, and the floating diffusion layer is formed to be exposed on the surface of the semiconductor substrate.

[Claim 2] The solid-state imaging apparatus according to claim 1, wherein an impurity concentration of the floating diffusion layer is lower than an impurity concentration of the source/drain diffusion layer of the

amplifier transistor.

[Claim 3] The solid-state imaging apparatus according to claim 1, wherein each of the photosensitive cells further includes a reset transistor for resetting the floating diffusion layer,

the driving means includes:

a vertical driver circuit for simultaneously driving the transfer transistor and the reset transistor in a vertical direction;

a noise suppressing circuit for obtaining a signal output to a plurality of vertical signal lines disposed in a vertical direction in the photosensitive region; and

a horizontal driver circuit provided for outputting a signal from the noise suppressing circuit in a time series by successively switching a plurality of horizontal transistors disposed in a horizontal direction, and

an impurity concentration of the floating diffusion layer is lower than an impurity concentration of a source/drain diffusion layer provided in a plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit.

[Claim 4] The solid-state imaging apparatus according to claim 3, wherein the source/drain diffusion layer provided in the plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit is covered with a salicide layer.

[Claim 5] The solid-state imaging apparatus according to claim 1, wherein the transfer transistor and the amplifier transistor are composed of an n-type MOS transistor.

[Claim 6] The solid-state imaging apparatus according to claim 3, wherein the vertical driver circuit and the horizontal driver circuit are composed of a dynamic logic circuit.

[Claim 7] The solid-state imaging apparatus according to claim 3, wherein an impurity concentration of a source/drain diffusion layer of a part of the plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit is lower than an impurity concentration of a source/drain diffusion layer of another part of the plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit.

[Claim 8] The solid-state imaging apparatus according to claim 3, wherein a source/drain diffusion layer of a part of the plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit is formed to be exposed on a surface of the semiconductor substrate, and a source/drain diffusion layer of another part of the plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit is covered with a salicide layer.

[Claim 9] The solid-state imaging apparatus according to claim 1, wherein an impurity concentration of the floating diffusion layer is 1×10^{18} cm^{-3} or less.

[Claim 10] A method for producing the solid-state imaging apparatus of claim 1 comprising the steps of:

forming the photodiode, the transfer transistor, and the amplifier transistor on the semiconductor substrate;

forming a resist into a predetermined pattern so as to cover the photodiode, the transfer transistor, and the amplifier transistor;

implanting ions into the semiconductor substrate using the resist as a mask so as to form the floating diffusion layer;

removing the resist and forming a salicide blocking film so as to cover the floating diffusion layer and the photodiode;

forming a source/drain diffusion layer of the amplifier transistor;

and

forming a salicide layer so as to cover the source/drain diffusion layer of the amplifier transistor.

[Claim 11] The solid-state imaging apparatus according to claim 10, wherein an impurity concentration of the floating diffusion layer is lower than an impurity concentration of the source/drain diffusion layer of the amplifier transistor.

[Claim 12] A method for producing the solid-state imaging apparatus of claim 1, comprising the steps of:

forming a resist in a predetermined pattern on the semiconductor substrate;

implanting ions using the resist as a mask so as to form the photodiode;

removing the resist and forming the transfer transistor and the amplifier transistor on the semiconductor substrate;

forming a first salicide blocking film so as to cover the photodiode;

implanting ions into the semiconductor substrate so as to form the floating diffusion layer and the source/drain diffusion layer of the amplifier transistor;

forming a second salicide blocking film so as to cover the floating diffusion layer; and

forming a salicide layer so as to cover the source/drain diffusion layer of the amplifier transistor.

[Claim 13] The solid-state imaging apparatus according to claim 12, wherein an impurity concentration of the floating diffusion layer is lower than an impurity concentration of the source/drain diffusion layer of the amplifier transistor.

[Detailed Description of the Invention]

[0001]

[Field of the Invention]

The present invention relates to a solid-state imaging apparatus equipped with an area image sensor used for a household video camera, a digital still camera, a camera for a mobile telephone, etc., and a method for producing the solid-state imaging apparatus.

[0002]

[Prior Art]

FIG. 13 is a circuit diagram showing a configuration of a conventional solid-state imaging apparatus 90. Photosensitive cells 98 composed of photodiodes 95, transfer gates 96, amplifier transistors 92, and reset transistors 97 are arranged in a matrix (3 row × 3 column).

[0003]

Drains of the amplifier transistor 92 and the reset transistor 97 are connected to a common drain line 306. A source of the amplifier transistor 92 is connected to a vertical signal line 15, as shown in FIG. 13. One end of the vertical signal line 15 is connected to a load transistor 305, and the other end thereof is connected to a noise suppressing circuit 12. Outputs of the noise suppressing circuit 12 are connected to horizontal transistors 14 driven by a horizontal driver circuit 13. Each photosensitive cell 98 is driven by a vertical driver circuit 11.

[0004]

FIG. 14 is plan view showing a configuration of the photosensitive cells 98 provided in the conventional solid-state imaging apparatus 90. A signal of the photodiode 95 is read to a floating diffusion layer 91 through the transfer gate 96. The signal that has been subjected to voltage

conversion in the floating diffusion layer 91 is applied from a floating diffusion layer contact 203 to a gate 304 of the amplifier transistor 92. A source/drain of the amplifier transistor 92 is connected to the common drain line 306 and the vertical signal line 15. A signal charge in the floating diffusion layer 91 is discharged to the common drain line 306 through the reset transistor 97.

[0005]

FIG. 15 is a cross-sectional view along a plane XYZW shown in FIG. 14. The photodiode 95 composed of an n-type photodiode diffusion layer 402 and a p-type leakage blocking layer 403 is formed in a P-type semiconductor substrate 9.

[0006]

A gate electrode of a MOS transistor constituting the transfer gate 96, the reset transistor 97, and the amplifier transistor 92 has a double-layered structure of a polysilicon layer 406 and a salicide layer 407.

[0007]

The floating diffusion layer 91 has the salicide layer 407 on a double diffusion layer composed of an LDD diffusion layer 404 and a source/drain diffusion layer 405.

[0008]

A source/drain of the MOS transistor has the salicide layer 407 on the double diffusion layer composed of the LDD diffusion layer 404 and the source/drain diffusion layer 405. The salicide layer 407 does not transmit light, so that it is removed from an upper portion of the photodiode 301.

[0009]

FIGS. 16 to 19 are cross-sectional views showing a method for producing the conventional solid-state imaging apparatus 90. As shown in

FIG. 16, after a device separating layer 502 is formed on a semiconductor substrate 9, a resist 501 is formed in a predetermined pattern by photoetching, and an n-type photodiode diffusion layer 402 and a p-type leakage blocking layer 403 are formed by ion implanting.

[0010]

After the resist 501 is removed, a polysilicon layer 406 to be gate electrodes of MOS transistors constituting the transfer gate 96, the reset transistor 97, and the amplifier transistor 92 is formed, as shown in FIG. 17. Thereafter, a salicide blocking film 503 is formed so as to cover the photodiode 95, and then, a LDD diffusion layer 404 is formed so as to be self-aligned with the polysilicon layer 406 by ion implanting.

[0011]

Then, as shown in FIG. 18, an LDD oxide film 504 is deposited so as to cover the salicide blocking film 503, the polysilicon film 406, and the LDD diffusion layer 404. Then, as shown in FIG. 19, the LDD oxide film 504 is removed by anisotropic etching, whereby parts of the LDD oxide film 504 remain on both sides of the polysilicon layer 406 deposited thick in a vertical direction. A source/drain diffusion layer 405 is formed so as to be self-aligned with the LDD oxide film. Thereafter, metal materials such as titanium (Ti), cobalt (Co), etc. are deposited by sputtering, followed by heating. As a result, only the portions where the semiconductor substrate and polysilicon are exposed are salicided, and a salicide layer 407 remains.

[0012]

[Patent Document 1]

JP 8-335688 A

[0013]

[Problems to be Solved by the Invention]

However, in the above-mentioned configuration of the photosensitive cells in the conventional solid-state imaging apparatus, the floating diffusion layer 91 temporarily accumulates a signal of the photodiode 95. At this time, when there is a pn-junction opposite-direction leakage current in the floating diffusion layer 91, the leakage current is superimposed on the signal to generate noise.

[0014]

The time for signal charge to remain is shorter than that for the photodiode 95 to subject incident light to photoelectric exchange and store it. Therefore, a requirement for a pn-junction opposite-direction leakage current is not so strict as in a photodiode; however, when the floating diffusion layer 91 is produced in the same way as in source/drain of other transistors, a pn-junction opposite-direction leakage current is increased and causes serious noise. When this noise is large, the sensitivity of the solid-state imaging apparatus is decreased to degrade an S/N ratio of a signal, etc.

[0015]

It is an object of the present invention to provide a solid-state imaging apparatus having small noise and high sensitivity, and a method for producing the same.

[0016]

[Means for Solving the Problems]

A solid-state imaging apparatus according to the present invention includes a plurality of photosensitive cells disposed in a matrix in a photosensitive region on a semiconductor substrate, and driving means for driving the plurality of photosensitive cells. Each of the photosensitive cells includes a photodiode formed to be exposed on a surface of the

semiconductor substrate, for accumulating signal charge obtained by subjecting incident light to photoelectric exchange, a transfer transistor formed on the semiconductor substrate for transferring the signal charge accumulated in the photodiode, a floating diffusion layer formed on the semiconductor substrate for temporarily accumulating the signal charge transferred by the transfer transistor, and an amplifier transistor formed on the semiconductor substrate, for amplifying the signal charge temporarily accumulated in the floating diffusion layer. A source/drain diffusion layer provided in the amplifier transistor is covered with a salicide layer, and the floating diffusion layer is formed to be exposed on the surface of the semiconductor substrate.

[0017]

A method for producing the above-mentioned solid-state imaging apparatus according to the present invention includes the steps of forming the photodiode, the transfer transistor, and the amplifier transistor on the semiconductor substrate, forming a resist in a predetermined pattern so as to cover the photodiode, the transfer transistor, and the amplifier transistor, implanting ions into the semiconductor substrate using the resist as a mask so as to form the floating diffusion layer, removing the resist and forming a salicide blocking film so as to cover the floating diffusion layer and the photodiode, forming a source/drain diffusion layer of the amplifier transistor, and forming a salicide layer so as to cover the source/drain diffusion layer of the amplifier transistor.

[0018]

Another method for producing the above-mentioned solid-state imaging apparatus according to the present invention includes the steps of forming a resist in a predetermined pattern on the semiconductor substrate,

implanting ions using the resist as a mask so as to form the photodiode, removing the resist and forming the transfer transistor and the amplifier transistor on the semiconductor substrate, forming a first salicide blocking film so as to cover the photodiode, implanting ions into the semiconductor substrate so as to form the floating diffusion layer and the source/drain diffusion layer of the amplifier transistor, forming a second salicide blocking film so as to cover the floating diffusion layer, and forming a salicide layer so as to cover the source/drain diffusion layer of the amplifier transistor.

[0019]

[Embodiments of the Invention]

In the solid-state imaging apparatus according to the present embodiment, the source/drain diffusion layer provided in the amplifier transistor is covered with a salicide layer, and the floating diffusion layer is formed so as to be exposed on a surface of the semiconductor substrate. Therefore, the salicide layer is not formed on the surface of the floating diffusion layer. Thus, a pn-junction opposite-direction leakage current is reduced in the floating diffusion layer. As a result, a solid-state imaging apparatus with small noise and high sensitivity can be obtained.

[0020]

In the present embodiment, it is preferable that an impurity concentration of the floating diffusion layer is lower than an impurity concentration of the source/drain diffusion layer of the amplifier transistor.

[0021]

It is preferable that each of the photosensitive cells further includes a reset transistor for resetting the floating diffusion layer. It also is preferable that the driving means includes a vertical driver circuit for simultaneously driving the transfer transistor and the reset transistor in a

vertical direction, a noise suppressing circuit for obtaining a signal output to a plurality of vertical signal lines disposed in a vertical direction in the photosensitive region, and a horizontal driver circuit for outputting a signal from the noise suppressing circuit in a time series by successively switching a plurality of horizontal transistors disposed in a horizontal direction. It also is preferable that an impurity concentration of the floating diffusion layer is lower than an impurity concentration of a source/drain diffusion layer provided in a plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit.

[0022]

It is preferable that the source/drain diffusion layer provided in the plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit is covered with a salicide layer.

[0023]

It is preferable that the transfer transistor and the amplifier transistor are composed of an n-type MOS transistor.

[0024]

It is preferable that the vertical driver circuit and the horizontal driver circuit are composed of a dynamic logic circuit.

[0025]

It is preferable that an impurity concentration of a source/drain diffusion layer of a part of the plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit is lower than an impurity concentration of a source/drain diffusion layer of another part of the plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit.

[0026]

It is preferable that a source/drain diffusion layer of a part of the plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit is formed to be exposed on a surface of the semiconductor substrate, and a source/drain diffusion layer of another part of the plurality of transistors constituting the vertical driver circuit and the horizontal driver circuit is covered with a salicide layer.

[0027]

It is preferable that an impurity concentration of the floating diffusion layer is 1×10^{18} cm^{-3} or less.

[0028]

A method for producing the solid-state imaging apparatus according to the present embodiment includes the steps of forming a salicide blocking film so as to cover a floating diffusion layer and a photodiode, forming a source/drain diffusion layer of an amplifier transistor, and forming a salicide layer so as to cover the source/drain diffusion layer of the amplifier transistor. Therefore, the salicide layer is not formed on the surface of the floating diffusion layer. Thus, in the floating diffusion layer, a pn-junction opposite-direction leakage current is reduced. As a result, a solid-state imaging apparatus with small noise and high sensitivity can be obtained.

[0029]

It is preferable that an impurity concentration of the floating diffusion layer is lower than an impurity concentration of the source/drain diffusion layer of the amplifier transistor.

[0030]

A method for producing the solid-state imaging apparatus according to another embodiment includes forming a second salicide blocking film so as to cover a floating diffusion layer, and forming a salicide layer so as to

cover a source/drain diffusion layer of an amplifier transistor. Therefore, the salicide layer is not formed on the surface of the floating diffusion layer. Thus, in the floating diffusion layer, a pn-junction opposite-direction leakage current is reduced. As a result, a solid-state imaging apparatus with small noise and high sensitivity can be obtained.

[0031]

Hereinafter, the present invention will be described by way of illustrative embodiments with reference to the drawings.

[0032]

FIG. 1 is a circuit diagram showing a configuration of a solid-state imaging apparatus 100 according to the present embodiment. Photosensitive cells 8 composed of photodiodes 5, transfer gates 6, amplifier transistors 2, and reset transistors 7 are arranged in a matrix (3 row × 3 column).

[0033]

Drains of the amplifier transistor 2 and the reset transistor 7 are connected to a common drain line 306. A source of the amplifier transistor 2 is connected to a vertical signal line 15, as shown in FIG. 1. One end of the vertical signal line 15 is connected to a load transistor 305, and the other end thereof is connected to a noise suppressing circuit 12. Outputs of the noise suppressing circuit 12 are connected to horizontal transistors 14 driven by a horizontal driver circuit 13. Each photosensitive cell 8 is driven by a vertical driver circuit 11.

[0034]

FIG. 2 is plan view showing a configuration of the photosensitive cells 8 provided in the solid-state imaging apparatus 100. A signal of the photodiode 5 is read to a floating diffusion layer 1 through the transfer gate

6. The signal that has been subjected to voltage conversion in the floating diffusion layer 1 is applied from a floating diffusion layer contact 203 to a gate 304 of the amplifier transistor 2. A source/drain of the amplifier transistor 2 is connected to the common drain line 306 and the vertical signal line 15. Signal charge in the floating diffusion layer 1 is discharged to the common drain line 306 through the reset transistor 7.

[0035]

FIGS. 3 to 5 are cross-sectional views showing a method for producing the solid-state imaging apparatus 100 according to the present embodiment. Referring to FIG. 3, a polysilicon layer 406 to be gate electrodes of MOS transistors constituting the transfer gate 6, the reset transistor 7, and the amplifier transistor 2 is formed. Thereafter, a resist 701 formed so as to open a portion to be a floating diffusion layer by photoetching is formed. Then, a low-concentration floating diffusion layer 1 is formed by ion implantation, using the resist 701 as a mask.

[0036]

Thereafter, as shown in FIG. 4, a salicide blocking film 503 is formed so as to cover the photodiode 5 and the floating diffusion layer 1.

[0037]

Then, as shown in FIG. 5, a source/drain layer 3 and a salicide layer 4 are formed by the same method as that of the above-mentioned prior art.

[0038]

FIG. 6 is a graph showing the frequency of a conjunction leakage current in the solid-state imaging apparatus 100. A horizontal axis represents the magnitude of a conjunction leakage current, and a vertical axis represents the number of pn-junction floating diffusion layers representing the junction leakage current of the horizontal axis. A solid

line 601 represents a distribution regarding the case where the salicide layer 4 is formed on the floating diffusion layer 1, and a dotted line 602 represents a distribution regarding the case where the salicide layer 4 is not formed on the floating diffusion layer 1. Compared with the case where the salicide layer 4 is not formed on the floating diffusion layer 1, the entire distribution is shifted to a larger conjunction leakage current in the case where the salicide layer 4 is formed on the floating diffusion layer 1. Furthermore, there is a distribution 603 in which a conjunction leakage current locally is very large. This leads to a point defect, resulting in a defective solid-state imaging apparatus.

[0039]

FIG. 7 is a graph showing a relationship between the impurity concentration and the conjunction leakage current of the floating diffusion layer 1 in the solid-state imaging apparatus 100. A horizontal axis represents the impurity concentration of the floating diffusion layer 1, and a vertical axis represents a conjunction leakage current. When the impurity concentration of the floating diffusion layer 1 reaches 1×10^{18} cm^{-3} or more, a conjunction leakage current is increased rapidly.

[0040]

As described above, according to the present embodiment, the source/drain diffusion layer 3 provided in the amplifier transistor 2 is covered with the salicide layer 4, and the floating diffusion layer 1 is formed so as to be exposed on the surface of the semiconductor substrate 9. Therefore, the salicide layer 4 is not formed on the surface of the floating diffusion layer 1. Thus, a pn-junction opposite-direction leakage current is reduced in the floating diffusion layer 1. As a result, a solid-state imaging apparatus with small noise and high sensitivity can be obtained.

[0041]

FIGS. 8 to 10 are cross-sectional views showing another method for producing a solid-state imaging apparatus according to the present embodiment. The same components as those described with reference to FIGS. 3 to 5 are denoted with the same reference numerals as those therein. Thus, the detailed description of these components will be omitted here.

[0042]

Referring to FIG. 8, an LDD diffusion layer is formed in the same way as in FIGS. 4 and 5 as described above. Referring to FIG. 9, a second salicide blocking film 801 is formed so as to cover a floating diffusion layer 1. Thereafter, as shown in FIG. 10, a source/drain layer 3 and a salicide layer 4 are formed in the same way as in the above prior art.

[0043]

FIG. 11 is a plan view showing a configuration of main portions of another solid-state imaging apparatus according to the present embodiment. The same components as those described with reference to FIG. 2 are denoted with the same reference numerals as those therein. Thus, the detailed description of the components will be omitted here.

[0044]

In the floating diffusion layer 1, instead of decreasing the impurity concentration of a diffusion layer by removing a salicide layer over an entire region, the salicide layer may be removed in a partial region to decrease the impurity concentration of the diffusion layer. In FIG. 11, it is effective to decrease the concentration by removing the salicide layer in a region other than a periphery 901 of a contact portion 203 of the floating diffusion layer 1.

[0045]

FIG. 12 is a circuit diagram showing a configuration of a dynamic logic circuit provided in the solid-state imaging apparatus according to the present embodiment. Recently, a CMOS logic has become mainstream of a semiconductor. Therefore, a MOS-type imaging apparatus often is configured using a CMOS logic. According to the CMOS logic, the steps are long and determined in view of miniaturization of a transistor, so that it is very difficult to change the steps due to a sensor.

[0046]

Particularly, in the miniaturized steps, a p-channel transistor is difficult to form. The reason for this is as follows: the mass of boron, which is a p-type impurity, is relatively low and the atoms are likely to move, so that it is difficult to produce a miniaturized transistor using boron. Therefore, in order to perform production steps peculiar to a sensor, using a miniaturized transistor, it is advantageous to configure a transistor only with a NMOS.

[0047]

When a circuit only with an NMOS is used, power consumption generally is increased compared with the case using a CMOS. Therefore, a dynamic logic circuit is used. The dynamic logic circuit performs an operation called booting for raising a voltage by the capacitance of a MOS. When a leakage current is increased, the MOS capacitance portion is not operated, either. This is exactly matched with the object of the present invention of decreasing a leakage current.

[0048]

Particularly, in an imaging apparatus applied to a recent digital still camera, there is a mode (long-duration exposure) for a very slow operation. Therefore, even in the NMOS dynamic logic circuit, it is necessary to

perform isolation of a low leakage current. FIG. 12 shows an example of a shift register circuit configured using a dynamic circuit. The description of the operation will be omitted here. When a leakage current of the MOS capacitance 902 is large, a slow operation cannot be performed. It is very effective to use isolation of the present invention for isolation of the MOS capacitance 902.

[0049]

More specifically, when the solid-state imaging apparatus is miniaturized, in establishing a low leakage current technique intended to provide higher performance such as element isolation, in order to exclude p–ch that makes it difficult to produce a miniaturized transistor to configure a transistor only with an N–chMOS, and to design a dynamic logic circuit for lower power consumption as in a CMOS, it is necessary to decrease a leakage current. A miniaturized transistor, a MOS only with n-channels, low leakage element isolation, and a dynamic logic circuit are the shortest route for realizing a solid-state imaging apparatus with high performance.

[0050]

[Effect of the Invention]

As described above, according to the present invention, a solid-state imaging apparatus with small noise and high sensitivity and a method for producing the same can be provided.

[Brief Description of the Drawings]

[FIG. 1] A circuit diagram showing a configuration of a solid-state imaging apparatus according to the present embodiment.

[FIG. 2] A plan view showing a configuration of main portions of the solid-state imaging apparatus according to the present embodiment.

[FIG. 3] A cross-sectional view showing a method for producing a

solid-state imaging apparatus according to the present embodiment.

[FIG. 4] A cross-sectional view showing the method for producing a solid-state imaging apparatus according to the present embodiment.

[FIG. 5] A cross-sectional view showing the method for producing a solid-state imaging apparatus according to the present embodiment.

[FIG. 6] A graph showing the frequency of a conjunction leakage current in the solid-state imaging apparatus according to the present embodiment.

[FIG. 7] A graph showing a relationship between an impurity concentration of a floating diffusion layer and a conjunction leakage current in the solid-state imaging apparatus according to the present embodiment.

[FIG. 8] A cross-sectional view showing another method for producing a solid-state imaging apparatus according to the present embodiment.

[FIG. 9] A cross-sectional view showing another method for producing a solid-state imaging apparatus according to the present embodiment.

[FIG. 10] A cross-sectional view showing another method for producing a solid-state imaging apparatus according to the present embodiment.

[FIG. 11] A plan view showing a configuration of main portions of another solid-state imaging apparatus according to the present embodiment.

[FIG. 12] A circuit diagram showing a configuration of a dynamic logic circuit provided in the solid-state imaging apparatus according to the present embodiment.

[FIG. 13] A circuit diagram showing a configuration of a conventional solid-state imaging apparatus.

[FIG. 14] A plan view showing a configuration of main portions of the conventional solid-state imaging apparatus.

[FIG. 15] A cross-sectional view showing a configuration of the conventional solid-state imaging apparatus.

[FIG. 16] A cross-sectional view showing a conventional method for producing a solid-state imaging apparatus.

[FIG. 17] A cross-sectional view showing the conventional method for producing a solid-state imaging apparatus.

[FIG. 18] A cross-sectional view showing the conventional method for producing a solid-state imaging apparatus.

[FIG. 19] A cross-sectional view showing the conventional method for producing a solid-state imaging apparatus.

[Description of the Reference Numerals]

1 Floating diffusion layer

2 Amplifier transistor

3 Source/drain layer

4 Salicide layer

5 Photodiode

6 Transfer transistor

7 Reset transistor

8 Photosensitive cell

9 Semiconductor substrate

11 Vertical driver

12 Noise suppressing circuit

13 Horizontal driver circuit

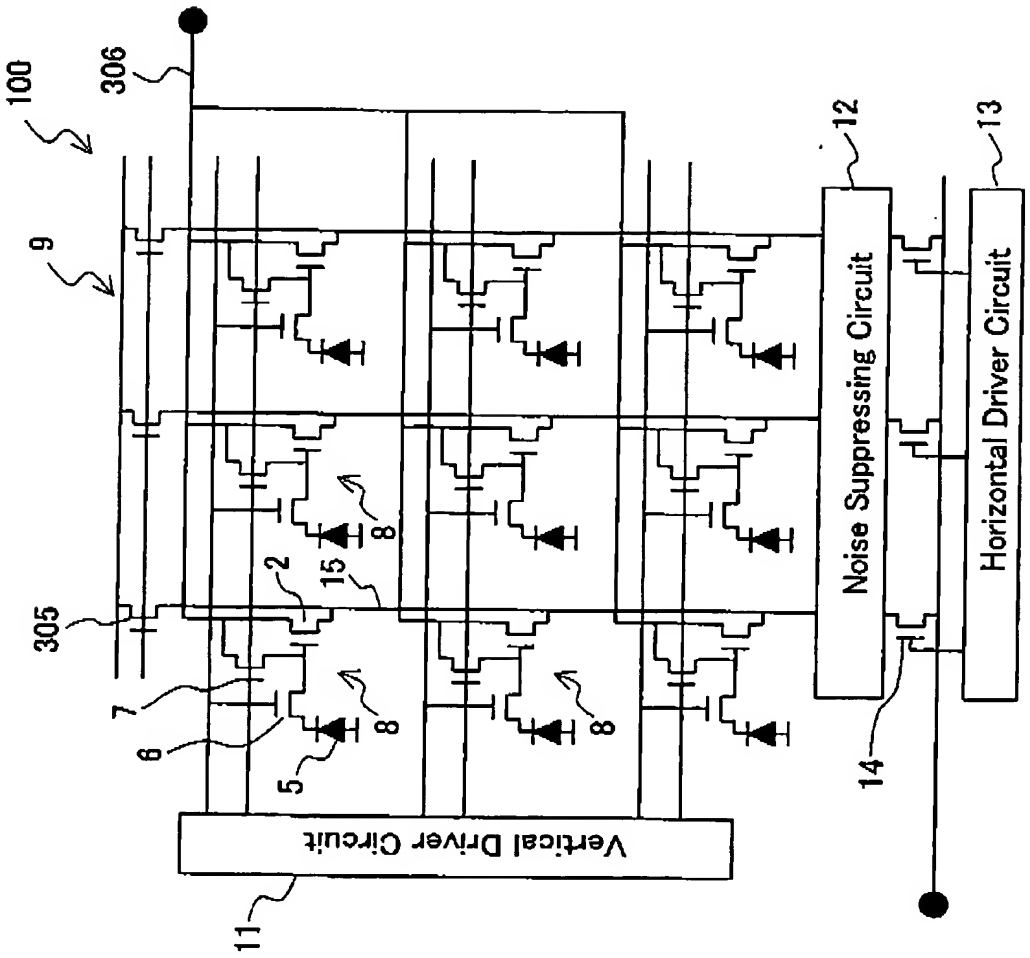
14 Horizontal transistor

15 Vertical signal line

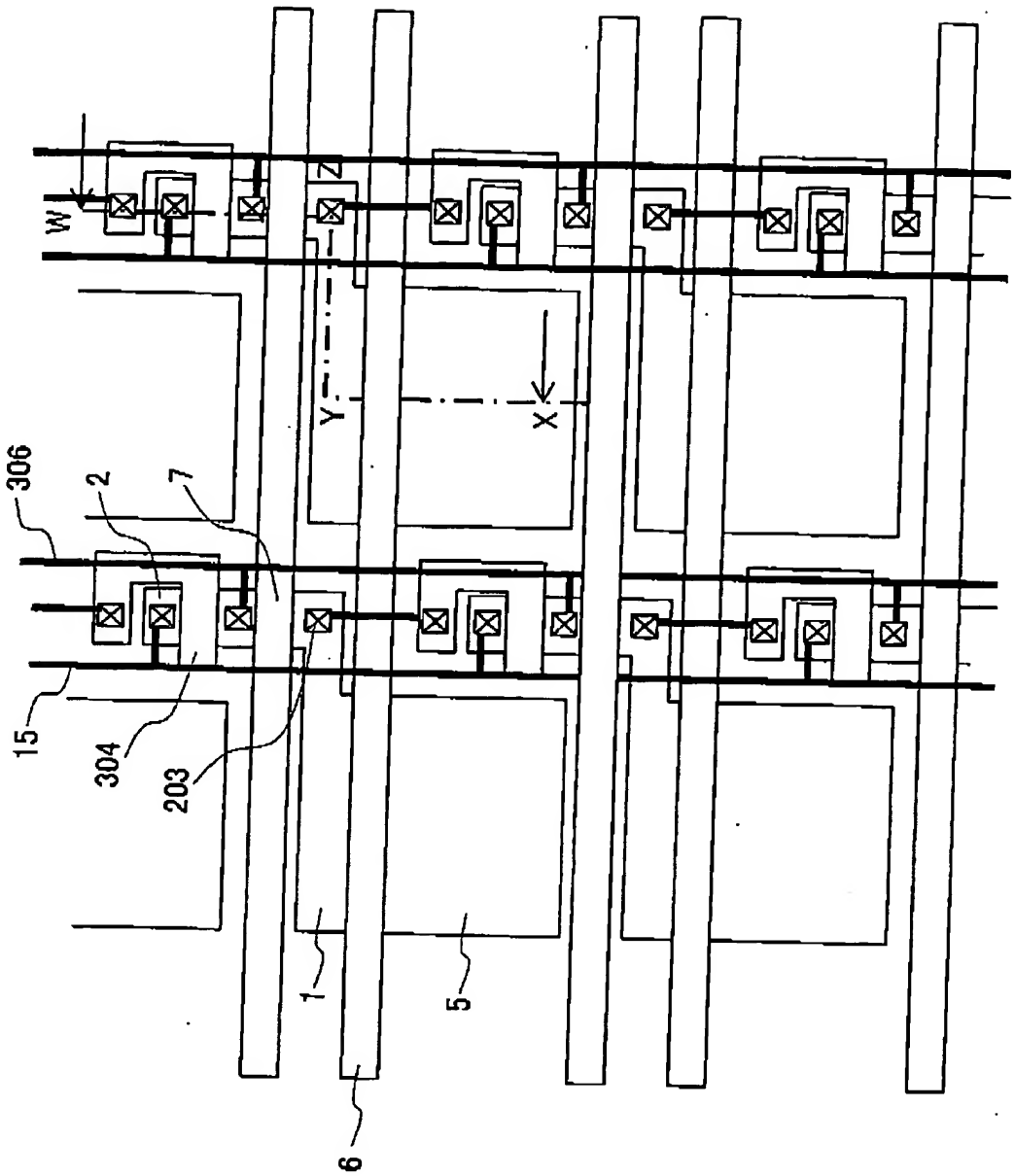
16 Dynamic logic circuit

100 Solid-state imaging apparatus

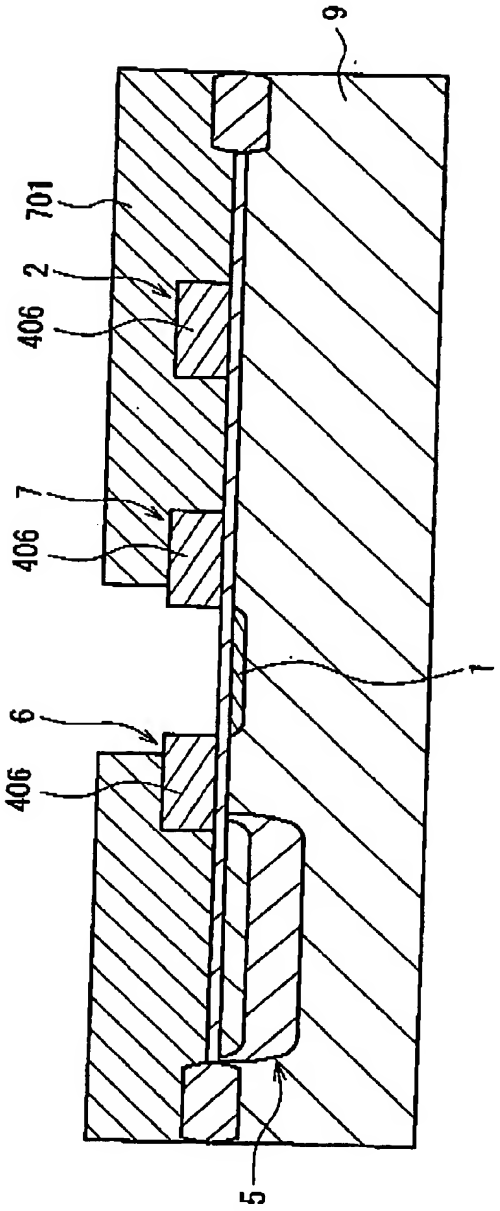
[Document Name] Drawings
[FIG. 1]



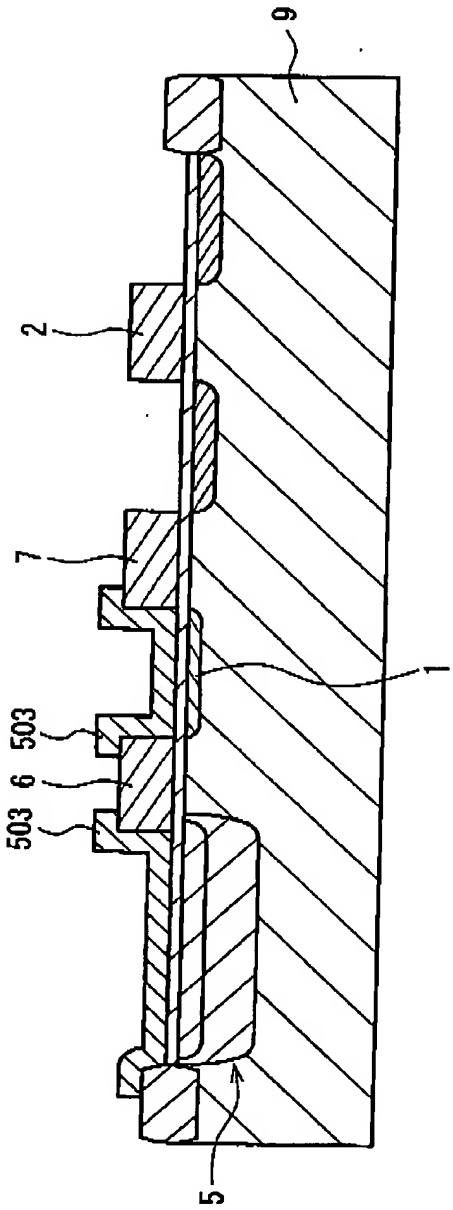
[FIG. 2]



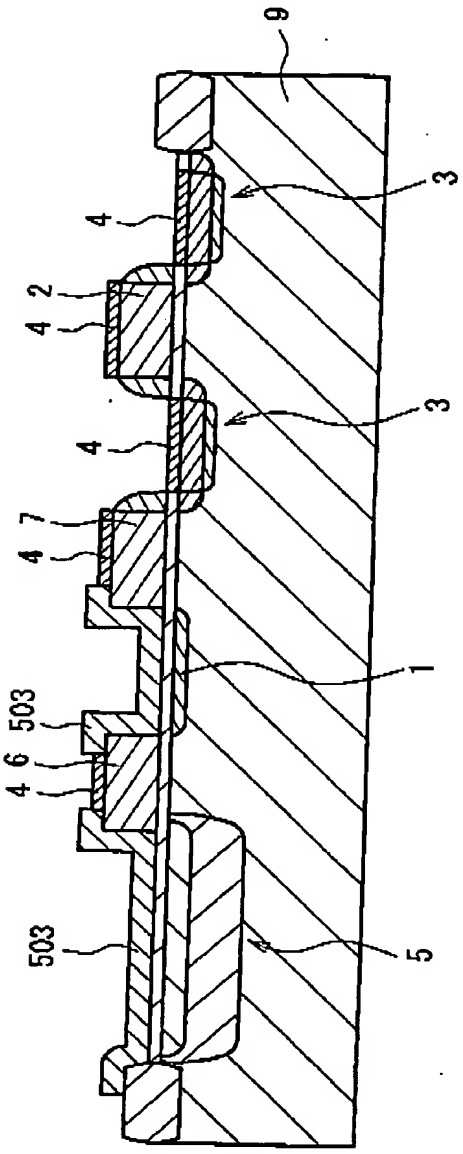
[FIG. 3]



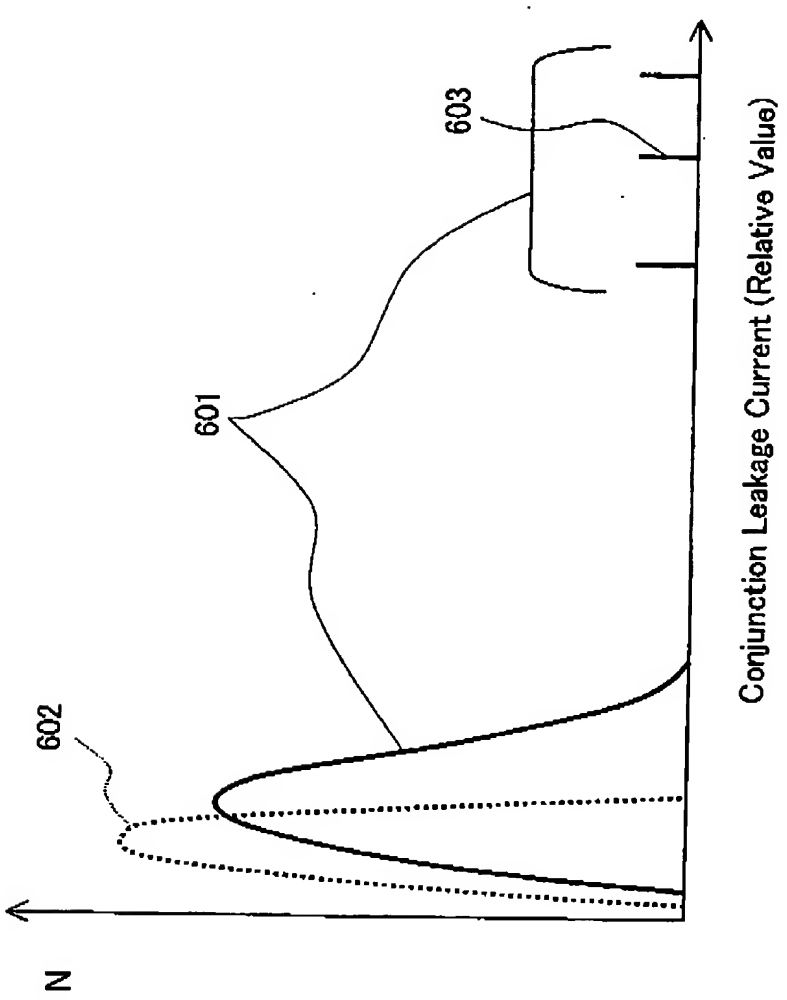
[FIG. 4]



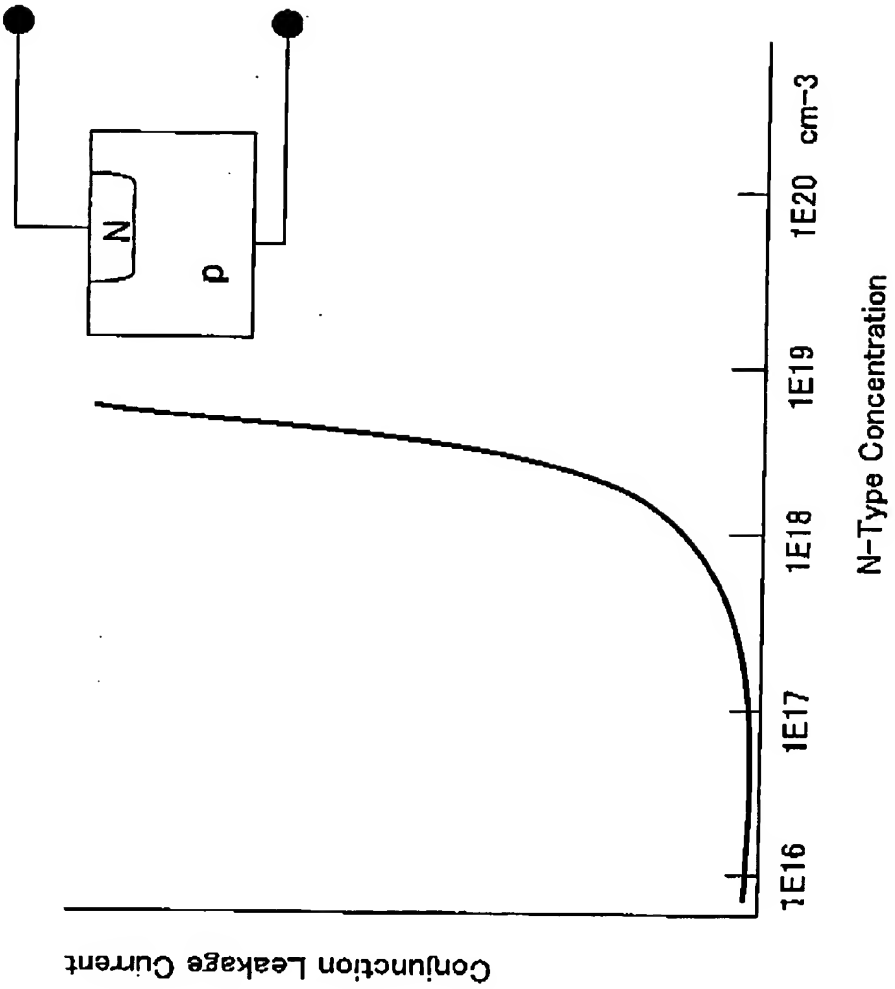
[FIG. 5]



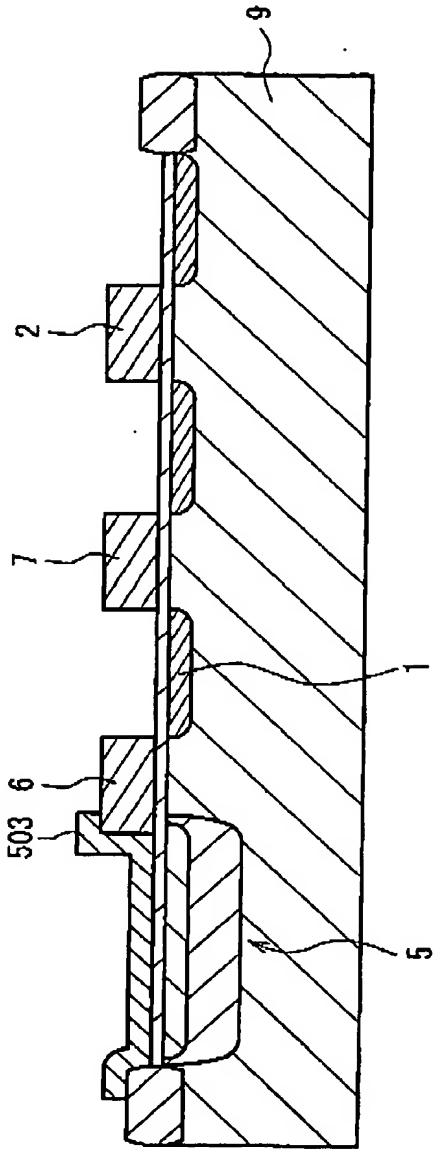
[FIG. 6]



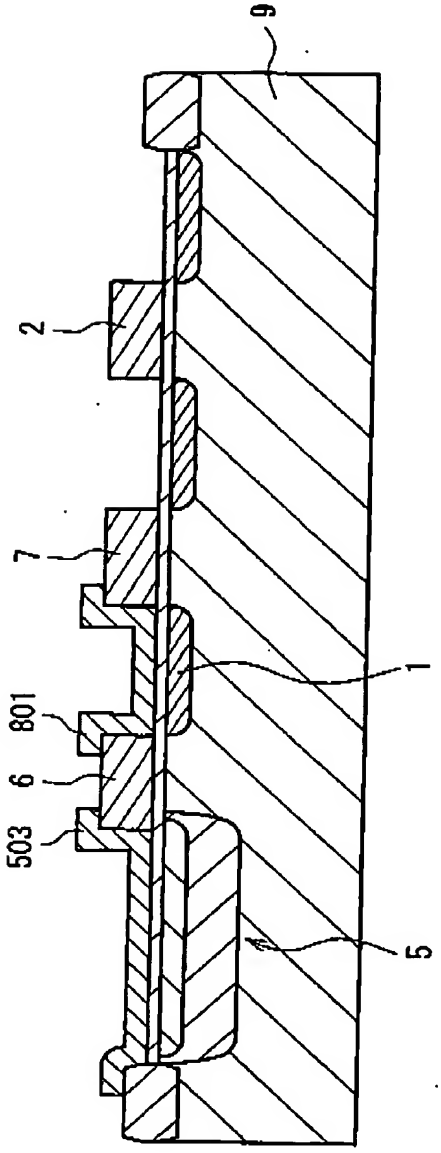
[FIG. 7]


N
p
1E16
1E17
1E18
1E19
1E20 cm-3
N-Type Concentration
Conjunction Leakage Current

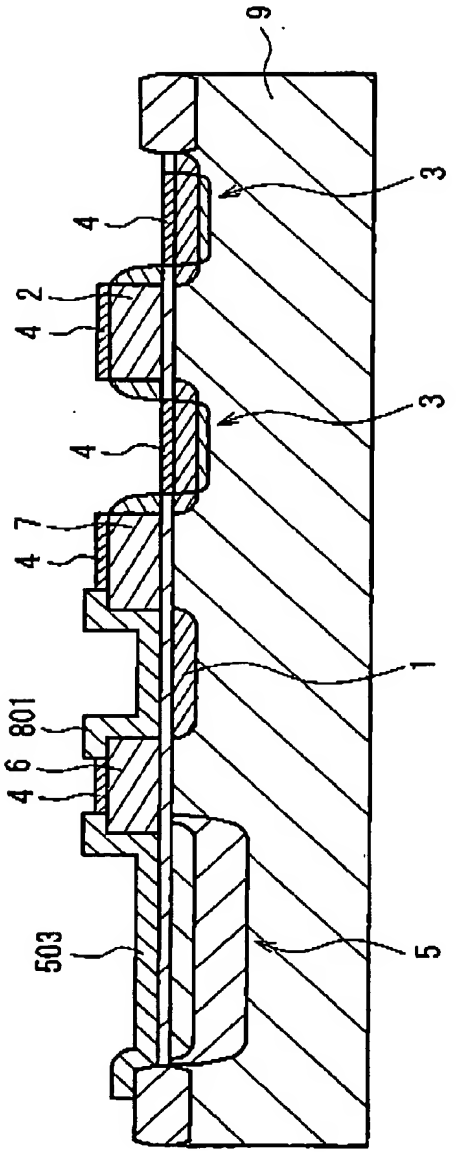
[FIG. 8]



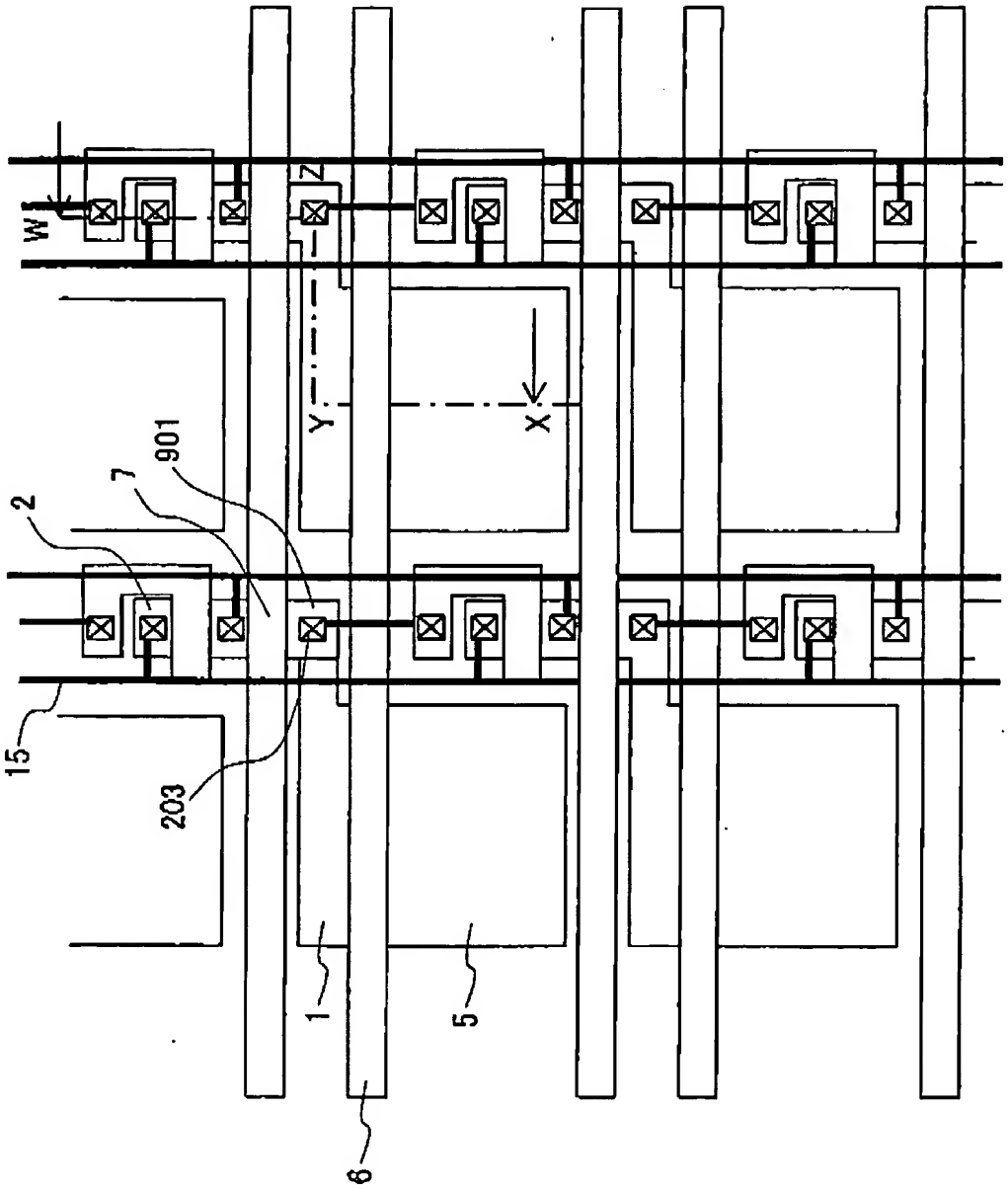
[FIG. 9]



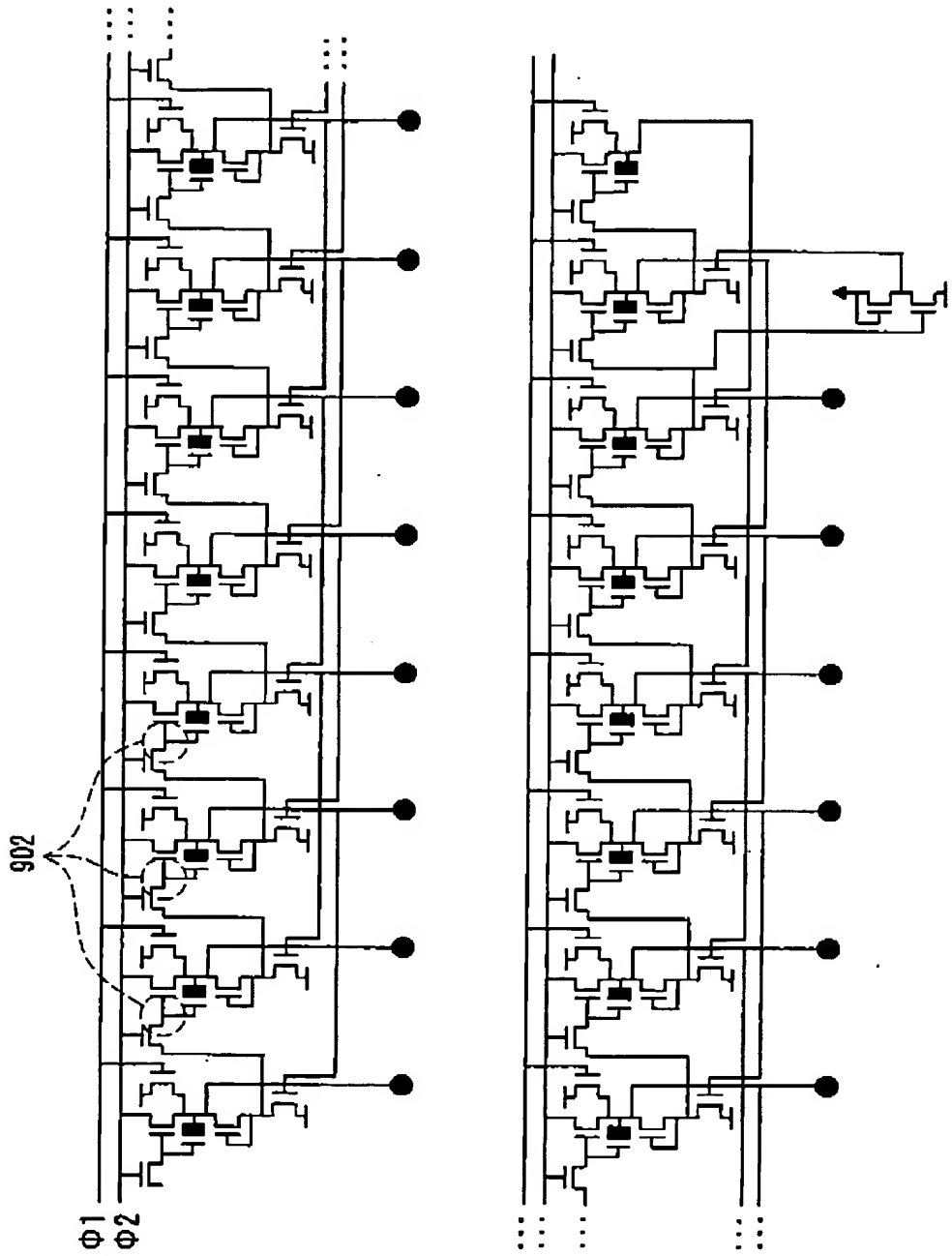
[FIG. 10]



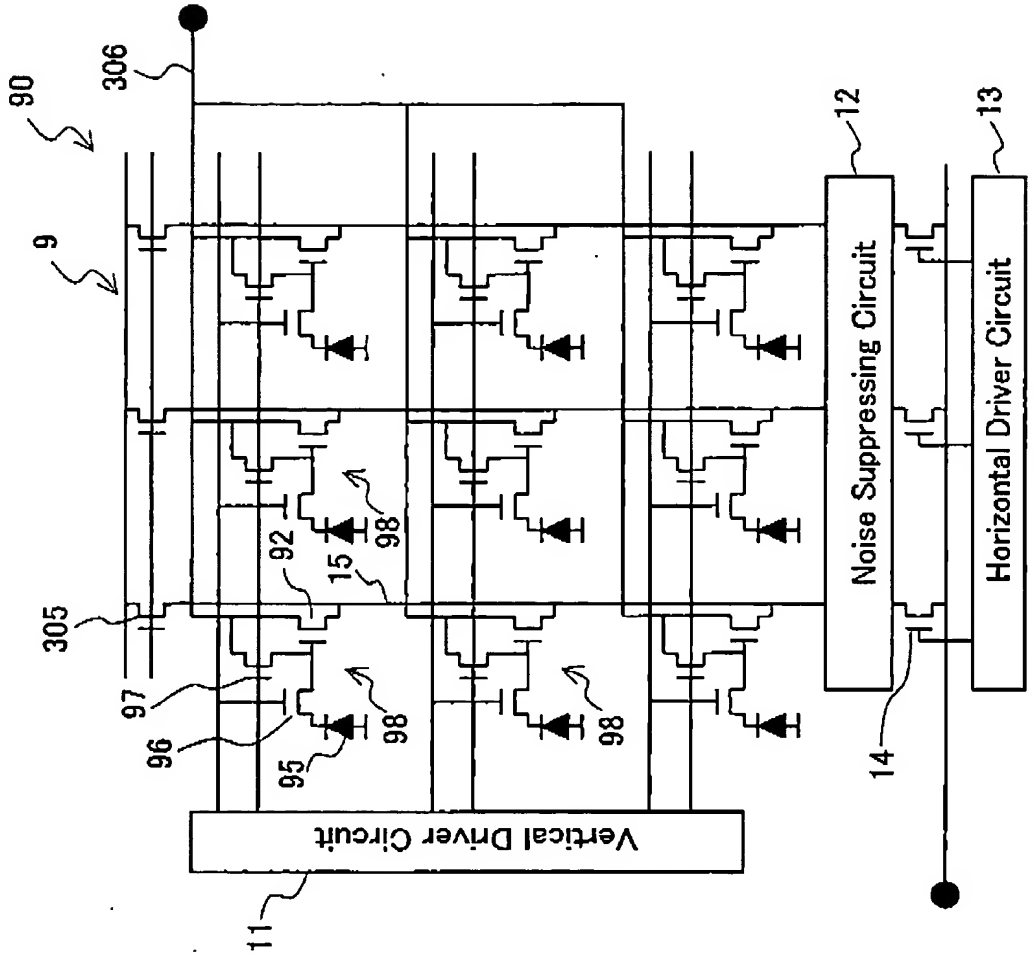
[FIG. 11]



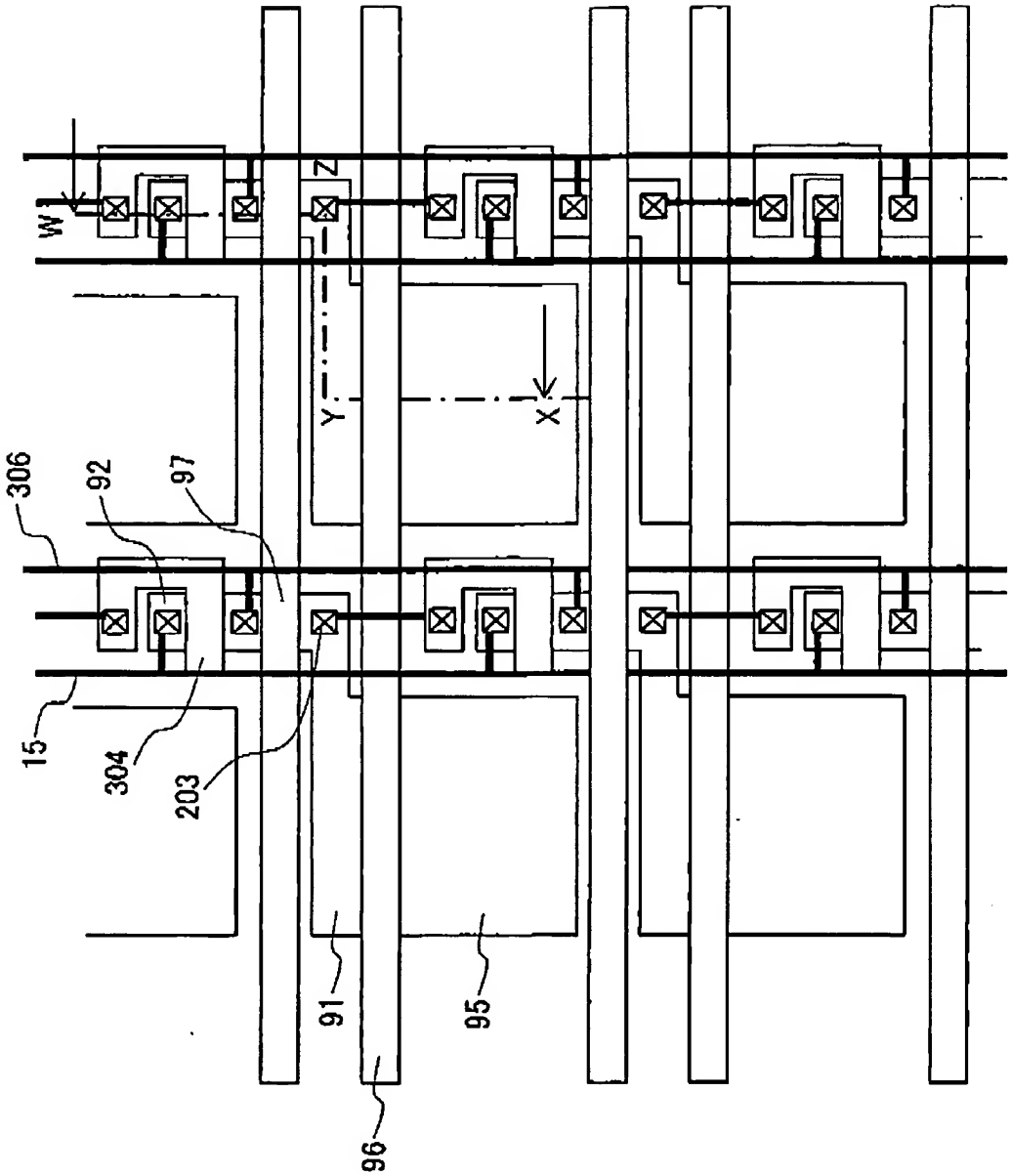
[FIG. 12]



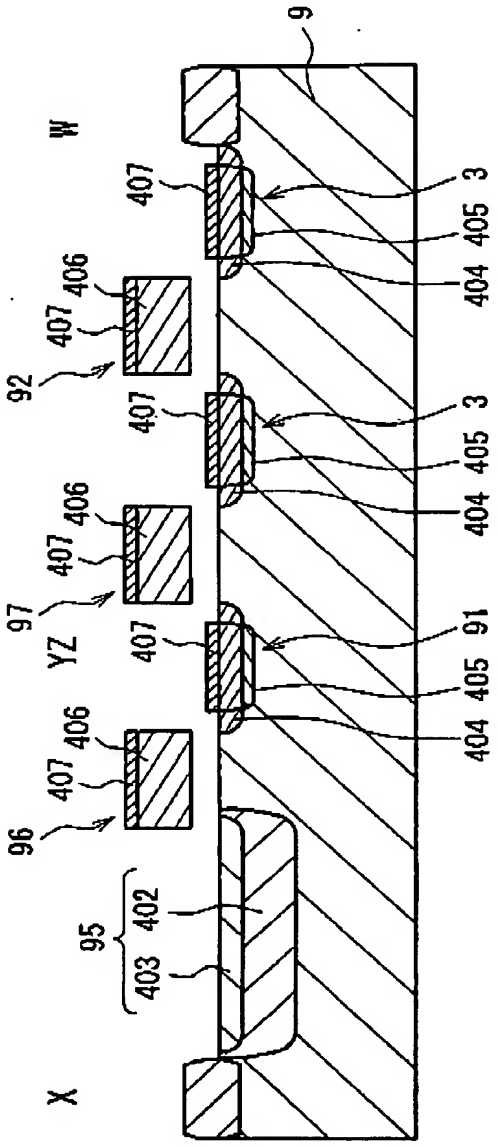
[FIG. 13]



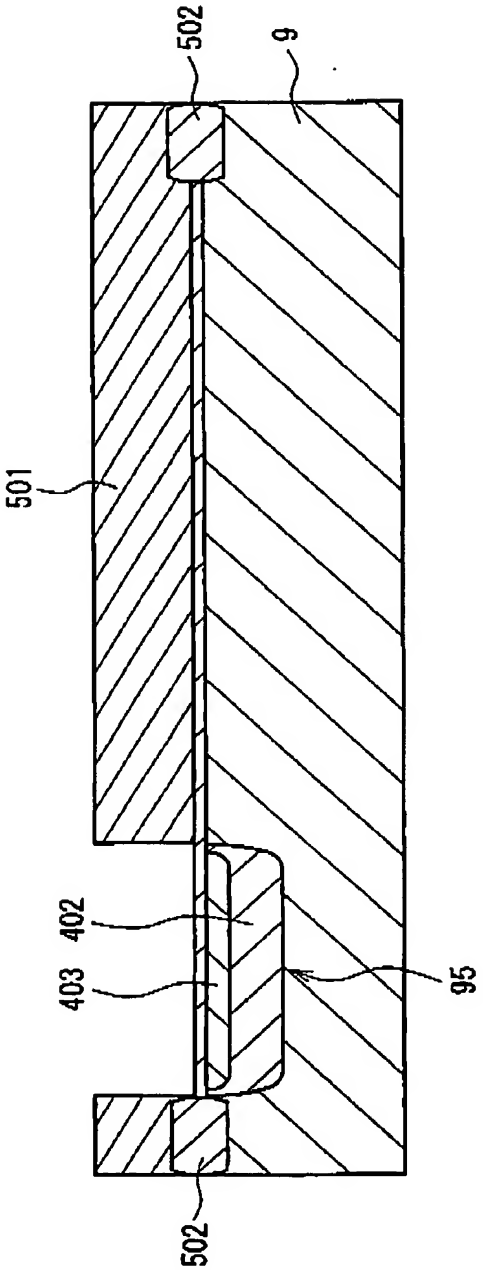
[FIG. 14]



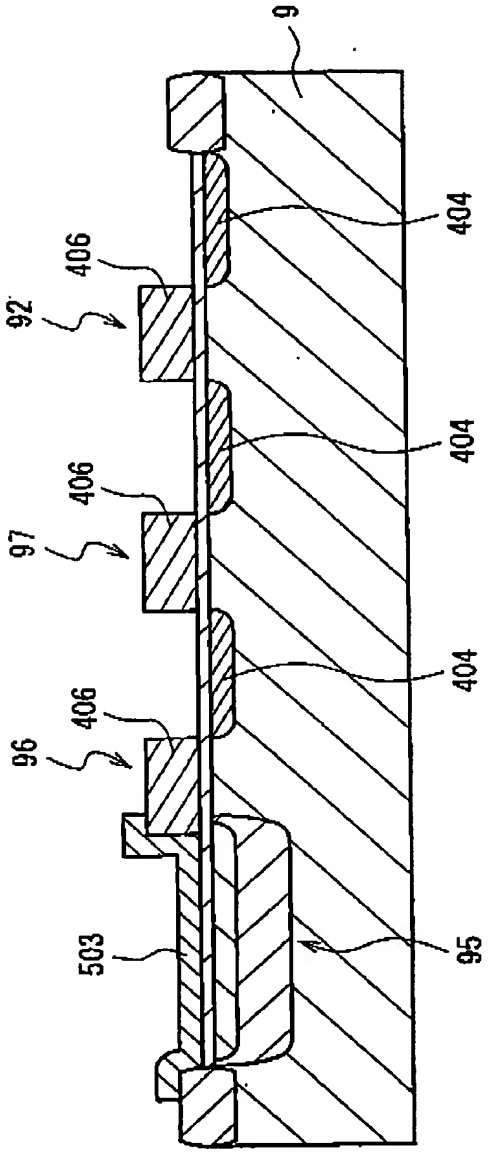
[FIG. 15]



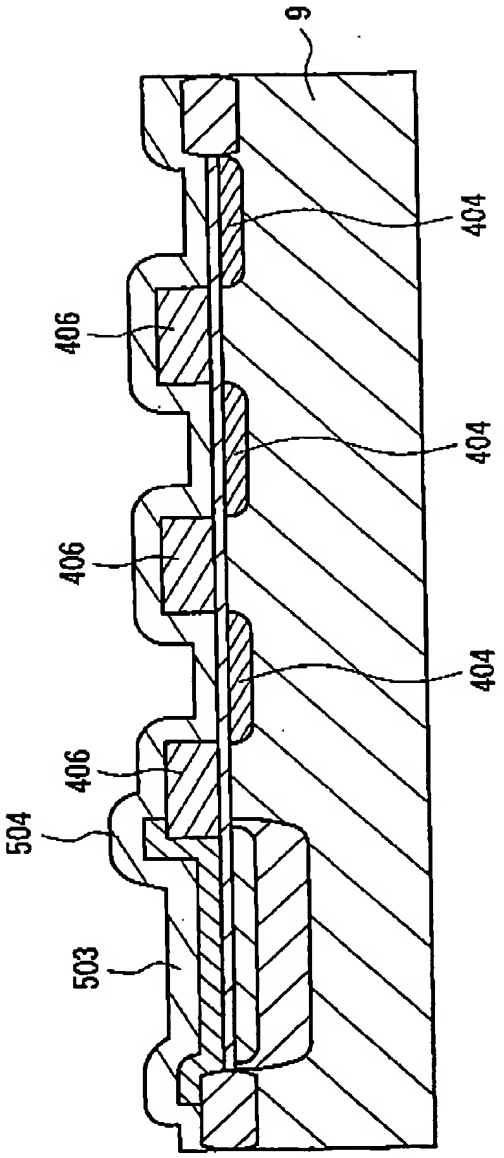
[FIG. 16]



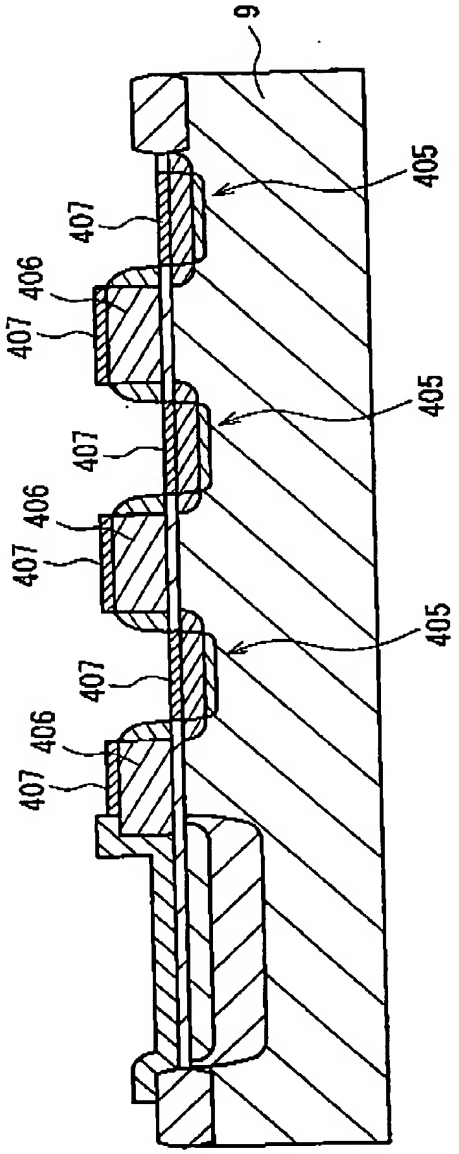
[FIG. 17]



[FIG. 18]



[FIG. 19]



[Name of the Document] ABSTRACT

[Abstract]

[Objective] A solid-state imaging apparatus with small noise and high sensitivity is provided.

[Means for Solving the Problem] A solid-state imaging apparatus includes a plurality of photosensitive cells, and driving means provided for driving the plurality of photosensitive cells. Each photosensitive cell includes a photodiode 5 formed to be exposed on a surface of a semiconductor substrate 9 for the purpose of accumulating signal charge obtained by subjecting incident light to photoelectric conversion, a transfer transistor 6 for transferring signal charge accumulated by the photodiode 5, a floating diffusion layer 1 for temporarily accumulating signal charge transferred by the transfer transistor 6, and an amplifier transistor 2 for amplifying signal charge temporarily accumulated in the floating diffusion layer 1. A source/drain diffusion layer 3 provided in the amplifier transistor 2 is covered with a salicide layer 4, and the floating diffusion layer 1 is formed to be exposed on a surface of the semiconductor substrate 9.

[Selected Figure] FIG. 5